UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ Specification — Total Pages 26
2. ☒ Drawing(s) (35USC 113) — Total Pages 3
3. ☒ Declaration and Power of Attorney — Total Pages 2
   a. ☒ Newly executed(original or copy)
   b. ☐ Copy from prior application (37CFR 1.63(d)) *(for continuation/divisional with Box 14 completed)* ***[Note Box 4 Below]***
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting Inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
4. ☐ Incorporation By Reference (usable if Box 3b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ACCOMPANYING APPLICATION PARTS

5. ☒ Assignment Papers (cover sheet & documentation) Sony Corporation
6. ☐ Letter under 37 CFR 1.41(c).
7. ☐ English Translation Document *(if applicable)*
8. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
9. ☐ Preliminary Amendment
10. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
11. ☐ Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
12. ☒ Certified Copy of Priority Document(s) Japanese P09-345363 filed 12-15-97
13. ☐ Other: _____

14. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) ☐ of prior application No: ___/

CLAIMS AS FILED

(1) FOR		(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) BASIC FEE $760.00
TOTAL CLAIMS	20	11	0	$18 00	
INDEPENDENT CLAIMS	03	1	0	$78 00	
		ANY MULTIPLE DEPENDENT CLAIMS? ☐ YES ☒NO		$260 00	
			TOTAL FILING FEE ->		$760.00

☒ The Commissioner is hereby authorized to charge any additional fees which may be required in connection with this application, or credit any overpayment to ACCOUNT NO. 08-2290. A duplicate copy of this sheet is enclosed.

☒ A check in the amount of $760.00 to cover the filing fee is enclosed.

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SIGNATURE: _____ **DATE:** **December 11, 1998**
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N 98 P121 ※※00

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, more specifically a complementary metal oxide semiconductor (CMOS) device having a p-channel MOS (hereafter called a PMOS) field effect transistor (FET) using holes as carriers and an n-channel MOS (hereafter called an NMOS) FET using electrons as carriers on the same chip.

2. Description of the Related Art

At the present time, most CMOS integrated circuits use a so-called two-layer "polycide" structure of a metal silicide layer and polycrystalline silicon layer for their gate electrodes so as to decrease the resistance of their gate electrodes.

In CMOS's having an NMOSFET and PMOSFET on the same substrate, it is generally known to use a so-called "dual gate" structure for the gate electrodes from the viewpoints of suppressing the short channel effect, controlling the threshold voltage, etc.

A CMOS having a dual gate structure is configured for example as shown in Fig. 1.

As shown in Fig. 1, element formation regions 104 and 105 at which the PMOS and NMOS are to be formed are enclosed by an element isolation region 103. A polycrystalline silicon layer 106 is formed on these element formation regions 104 and 105 over the element isolation region 103.

A p^+-type impurity is doped in the region of the polycrystalline silicon interconnection layer 106 over the element formation region 104 for forming the PMOS, while an n^+-type impurity is doped in the region of the polycrystalline silicon interconnection layer 106 over the element formation region 105 for forming the NMOS. These doped regions are thereby made conductive and form gate electrodes 101 and 102. Note that the gate electrodes 101 and 102 are electrically connected with each other by a metal silicide layer formed on the polycrystalline silicon interconnection layer 106 in a later step.

In the CMOS illustrated in Fig. 1, the impurities doped in the gate electrodes 101 and 102 tend to diffuse into the region 106a of the polycrystalline silicon layer 106 not doped with impurities.

If impurities diffuse into the region 106a, the impurities doped in the gate electrodes 101 and 102

will be depleted, the density of the impurities at the gate electrodes will fall, the change in the threshold voltage V_{th} and a fall in the current I_{DS} between the drain and source due to depletion of the gate electrodes will be caused.

To prevent a fall in the current I_{ds} between the drain and source, for example, a CMOS having the structure shown in Fig. 2 has been proposed.

In the CMOS shown in Fig. 2, the gate electrode 101 doped with the p^+-type impurity and the gate electrode 102 doped with the n^+-type impurity are formed over the element formation regions 104 and 105 and extending off over the element isolation region 103.

That is, when forming the gate electrodes 101 and 102 doping impurities, the impurities are doped in the polycrystalline silicon layer 106 so as to extend off by lengths L_{diff} from the element formation regions 104 and 105.

Accordingly, the extended regions 101a and 102a become sources of stored impurities.

Note that the width 2 x L_{ovlp} of the region 106a of the polycrystalline silicon interconnection layer 106 which is not doped with an impurity is a margin of safety set in view of possible mask

misalignment at the time of ion implantation of impurities into the polycrystalline silicon interconnection layer 106.

The length L_{diff} is the length required to prevent a drop in the density of impurities in the gate electrodes 101 and 102.

Accordingly, the drop of the density of impurities in the gate electrodes 101 and 102 can be considerably suppressed and a drop of the current I_{DS} between the drain and source can be prevented.

The problem is that, in the CMOS shown in Fig. 2, the distance L_p between the element formation regions 104 and 105 for forming the PMOS and NMOS becomes $2 \times (L_{diff} + L_{ovlp})$.

To make the extended regions suitably function as sources of stored impurities, the certain extent of the length L_{diff} is needed, for example, if L_g is 0.2 μm, L_{diff} must be 0.3 μm.

Thus, it is difficult to shorten the distance L_p between the PMOS and NMOS to further reduce the chip area.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a CMOS device having a dual gate structure suppressing lateral diffusion of the impurities doped in the n-type

and p-type gate electrodes, further shortening the distance between the PMOS and NMOS, and enabling further reduction of the chip size.

According to the present invention, there is provided a semiconductor device comprising a first element formation region in which a device of a first conductivity type is formed; a second element formation region separated from the first element formation region by an element isolation region and in which a device of a second conductivity type different from the first conductivity type is formed; a first gate electrode provided on the first element formation region and containing an impurity of the first conductivity type; a second gate electrode provided on the second element formation region facing the first gate electrode and containing an impurity of the second conductivity type; a first impurity storage region containing the first conductivity type impurity, having one end connected to an end of the first gate electrode, and arranged in a direction different from the direction of arrangement of the first and second gate electrodes; and a second impurity storage region containing the second conductivity type impurity, having one end connected to an end of the second gate electrode, having the other end electrically connected

to the other end of the first impurity storage region, and arranged in a direction different from the direction of arrangement of the first and second gate electrodes.

Preferably, the first and second impurity storage regions are physically connected to each other by a semiconductor layer.

More preferably, the semiconductor layer is formed by polycrystalline silicon and the first and second gate electrodes and first and second impurity storage regions are formed by selectively implanting impurities to the polycrystalline silicon layer.

Alternatively, more preferably the width of the semiconductor layer physically connecting the first and second impurity storage regions is a value allowing mask misalignment when forming the first and second gate electrodes and first and second impurity storage regions.

Alternatively, preferably the other ends of the first and second impurity storage regions are electrically connected to each other through a conductive layer.

Alternatively, preferably the first and second impurity storage regions are arranged in a direction perpendicular to the direction of arrangement of the

first and second gate electrodes.

Alternatively, preferably the first and second gate electrodes and the first and second impurity storage regions are formed in the same conductive semiconductor layer.

Alternatively, preferably a semiconductor device as set forth in claim 1, wherein the element isolation region is buried in a trench formed a boundary between the first and second conductive type of element formation regions in a semiconductor substrate.

Alternatively, preferably the element isolation region isolates first and second element formation regions comprised of semiconductor layers formed on an insulation layer.

More preferably, the element isolation region is buried in a trench formed in the semiconductor layers.

Alternatively, preferably the widths of the first and second impurity storage regions are equal to the gate length of the first and second gate electrodes and the lengths of the first and second impurity storage regions are longer than the gate length.

In the semiconductor device according to the present invention, by providing the first impurity storage region connected to the first gate electrode outside the first element formation region, the

difference in impurity density between the first gate electrode and the first impurity storage region is eliminated and the diffusion of the impurity from the first gate electrode is suppressed.

Similarly, by providing the second impurity storage region connected to the second gate electrode outside the second element formation region, the difference in impurity density between the second gate electrode and the second impurity storage region is eliminated and the diffusion of the impurity from the second gate electrode is suppressed.

Further, the first and second impurity storage regions connected to the first and second gate electrodes are arranged in a direction different from the direction of arrangement of the first and second gate electrodes and front ends of the two are connected electrically.

Accordingly, compared with arranging first and second impurity storage regions of the same length along the direction of arrangement of the first and second gate electrodes, it becomes possible to make the first and second element formation regions closer to each other. In the case of a CMOS, the distance between the PMOS and NMOS can be shortened to reduce the size of the semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become clearer from the following description of the preferred embodiments given with reference to the accompanying drawings, in which:

Fig. 1 is a view of an example of the gate electrode structure of a CMOS having a dual gate structure of the related art;

Fig. 2 is a view of another example of the gate electrode structure of a CMOS having a dual gate structure of the related art;

Fig. 3 is a view of an embodiment of the structure of gate electrodes of a semiconductor device according to the present invention;

Fig. 4 is a sectional view of a semiconductor device having the gate electrode structure illustrated in Fig. 3 in the A-A line direction and illustrates an example of a semiconductor device having a structure enabling shortening of the width of the element isolation region along with the shortening of the distance L_p between a PMOS formation region 4 and an NMOS formation region 5, and

Fig. 5 is a sectional view of the semiconductor device having the gate electrode structure illustrated

in Fig. 3 in the A-A line direction illustrating another example of a semiconductor device having a structure enabling shortening of the width of the element isolation region along with the shortening of the distance L_p between a PMOS formation region 4 and an NMOS formation region 5.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Below, a detailed explanation will be given of preferred embodiments of the present invention with reference to the drawings.

First Embodiment

Figure 3 is a view of an embodiment of the structure of gate electrodes of a semiconductor device according to the present invention.

As illustrated in Fig. 3, a PMOS formation region 4 for forming a PMOS and an NMOS formation region 5 for forming an NMOS are arranged apart from each other by a distance L_p.

On the PMOS formation region 4 is provided a p-type gate electrode 2 having a gate length L_g and a gate width L_w formed by doping a p^+-type impurity into a polycrystalline silicon layer 1.

On the NMOS formation region 5 is provided an n-type gate electrode 3 having a gate length L_g and a

gate width L_w formed by doping an n^+-type impurity into the polycrystalline silicon layer 1. This faces to p-type gate electrode 2 in the direction of arrangement of the p-type gate electrode 2.

Note that while the NMOS and PMOS are shown with the same gate widths L_w, generally the dimensions of the two differ.

Further, there is an element isolation region 7 between PMOS formation region 4 and NMOS formation region 5.

Note that, while not illustrated, a tungsten silicide or other metal silicide layer is formed by the self-aligned silicate technique on the polycrystalline silicon layer 1 and electrically connects the p-type gate electrode 2 and n-type gate electrode 3.

Outside the PMOS formation region 4, a p-type impurity storage region 6 is formed perpendicular to the direction of the gate width L_w of the p-type gate electrode 2.

The length of p-type impurity storage region 6 is $L_H + L_g$. The width is equal to the gate length L_g. One end is connected to the p-type gate electrode 2, while the other end is connected to the polycrystalline silicon interconnection layer 10.

Outside the NMOS formation region 5, an n-type

impurity storage region 8 is formed perpendicular to the direction of the gate width L_W of the n-type gate electrode 3.

The length of n-type impurity storage region 8 is $L_H + L_g$. The width is equal to the gate length L_g. One end is connected to the n-type gate electrode 3, while the other end is connected to the polycrystalline silicon interconnection layer 10.

The p-type gate electrode 2, the n-type gate electrode 3, the p-type impurity storage region 5, the n-type impurity storage region 8, and the polycrystalline silicon interconnection layer 10 are formed in the same polycrystalline silicon layer 1.

The p-type gate electrode 2 and the p-type impurity storage region 6 are formed by selective ion implantation of a p^+-type impurity into a predetermined region of the polycrystalline silicon layer 1.

The p^+-type impurity is, for example, boron fluoride ions (BF_2^+) and is implanted by a predetermined energy and dosage.

The n-type gate electrode 3 and n-type impurity storage region 8 are formed by selective ion implantation of an n^+-type impurity into a predetermined region of the polycrystalline silicon layer 1.

The n^+-type impurity is, for example, arsenic ions and is implanted by a predetermined energy and dosage.

The polycrystalline silicon interconnection layer 10 physically connects the front ends of the p-type impurity storage region 6 and the n-type impurity storage region 8.

The distance between the front ends of the p-type impurity storage region 6 and n-type impurity storage region is 2 x L_{ovlp}.

The part of the polycrystalline silicon interconnection layer 10 of the distance 2 x L_{ovlp} is the safety margin set in consideration of possible mask misalignment at the time of the selective ion implantation of impurities into the p-type gate electrode 2, the p-type impurity storage region 6, the n-type gate electrode 3, and the n-type impurity storage region 8.

That is, the masks used for the ion implantation into the p-type gate electrode 2 and the p-type impurity storage region 6 and into the n-type gate electrode 3 and n-type impurity storage region 8 are formed up to the broken line shown in Fig. 3 and are formed so as not to overlap at the broken line region.

By implanting p^+-type and n^+-type impurities into the p-type impurity storage region 6 and the n-type

impurity storage region 8, respectively, the p-type impurity storage region 6 and the n-type impurity storage region become kinds of sources of stored impurities.

That is, since impurities are implanted into the p-type impurity storage region 6 and n-type impurity storage region 8 at a similar density to the p-type gate electrode 2 and the n-type electrode 3, the lateral diffusion of impurities from p-type gate electrode 2 and n-type gate electrode 3 into the p-type impurity storage region 6 and n-type impurity storage region 8 is suppressed.

Accordingly, the drop of the densities of impurities in the p-type gate electrode 2 and n-type gate electrode 3 is suppressed, the change of threshold voltage V_{th} and the drop in current I_{ds} between the drain and source due to the depletion of the gates can be prevented.

In the gate structure according this embodiment, the p-type impurity storage region 6 and n-type impurity storage region 8 are formed in a direction perpendicular to the p-type gate electrode 2 and the n-type gate electrode 3. Thus, even if the effective length L_H of the p-type impurity storage region and n-type impurity storage region is changed as appropriate,

there is no need to change of the distance between the PMOS formation region 4 and NMOS formation region 5.

Further, in this embodiment, the effective length L_H of the p-type impurity storage region 6 and n-type impurity storage region 8 is set to at least the length L_{diff} of the regions 101a and 102a illustrated in Fig. 2. For example, the length L_H is so set that the shortest distance from ends of the gate electrodes 2, 3 on the PMOS formation region 4 and the NMOS formation region 5 to the polycrystalline silicon interconnection layer 10 become about the length L_{diff}.

Accordingly, the impurity storage region according to this embodiment give a similar performance with the impurity storage region of the gate electrode structure of the related art illustrated in Fig. 2 when the rest of the structure is the same.

The distance between the PMOS formation region 4 and NMOS formation region 5 in this embodiment is shown by the following equation (1):

$$L_p = 2 \times L_g + 2 \times L_{ovlp} \qquad (1)$$

Generally, the gate length L_g is shorter than the length L_{diff} required for the impurity storage region.

Thus, according to this embodiment, the distance L_p between the PMOS formation region 4 and the NMOS

formation region 5 can be made shorter than the distance L_p between the PMOS formation region 4 and NMOS formation region 5 of the gate electrode structure of the related art illustrated in Fig. 2.

As an actual example, when L_g = 0.20 μm, L_{ovlp} = 0.10 μm, and L_{diff} = 0.3 μm, L_p becomes 0.8 μm in the gate electrode structure of the related art but becomes 0.60 μm in this embodiment or 0.2 μm shorter.

Therefore, it is possible to reduce the chip area in a semiconductor chip formed with larger numbers of PMOS and NMOS devices.

Note that in this embodiment, the p-type impurity storage region 6 and n-type impurity storage region 8 were arranged outside the PMOS formation region 4 and NMOS formation region 5, but the present invention is not limited to this.

That is, it is possible to arrange the p-type impurity storage region 6 and n-type impurity storage region 8 at positions straddling the PMOS formation region 4 and NMOS formation region 5 and the element isolation region 7 and possible to form them inside the PMOS formation region 4 and NMOS formation region 5.

Further, in this embodiment, the p-type impurity storage region 6 and n-type impurity storage region 8 were arranged in a direction perpendicular to the p-

type gate electrode 2 and the n-type gate electrode 3, but the present invention is not limited to this.

That is , it is possible to arrange them not perpendicular to the direction of arrangement of the p-type gate electrode 2 and n-type electrode 3, but at a slant with respect to that direction.

Next, a specific example will be given of the effective range of the gate electrode structure of the above embodiment in relation to the element isolation region 7.

It is possible to shorten the distance L_p between the PMOS formation region 4 and NMOS formation region 5 by using the gate electrode structure according to the above embodiment.

To actually shorten the distance L_p, however, the element isolation width L_{iso} of the element isolation region 7 separating the PMOS formation region 4 and NMOS formation region 5 also has to be capable of being shortened.

Specifically, if the element isolation width L_{iso} satisfies at least the condition shown in the following relation (2), it is possible to shorten the distance L_p between the element formation regions by using the gate electrode structure of the above embodiment:

$$L_{iso} < 2 \times L_{diff} + 2 \times L_{ovlp} \qquad (2)$$

Here, Fig. 4 is a sectional view of a semiconductor device having the gate electrode illustrated in Fig. 3 along the A-A line direction and illustrates an example of a semiconductor device having a structure enabling the width of the element isolation region to be shortened along with the shortening of the distance L_p between the PMOS formation region 4 and NMOS formation region 5.

As illustrated in Fig. 4, a P-well 11 and an N-well 12 are formed in a silicon substrate 20. A trench element isolation region 7 comprised, for example, of silicon oxide is buried in a trench 13a formed in the silicon substrate 20 so as to straddle the P-well 11 and N-well 12.

A p-type gate electrode 2 and n-type gate electrode 3 are formed on the silicon substrate 20 through the insulation film 15, while a p-type impurity storage region 6, n-type impurity storage region 8, and polycrystalline silicon interconnection layer 10 are formed on the element isolation region 7.

L_{iso} in the figure is the element isolation width of the trench element isolation region 7.

Generally, it is known that the element isolation width L_{iso} can be made comparatively smaller since the trench element isolation region is buried in the

trench. Note that the method used for formation of the trench element isolation region 7 may be a generally known method, so an explanation of the method will be omitted.

Specifically, under the conditions of L_g = 0.20 μm, L_{ovlp} = 0.1 μm, and L_{diff} = 0.3 μm in the above embodiment, it is possible to make L_{iso} about 0.40 μm.

Thus, since the width L_p between the element formation regions in the case of the gate electrode structure of the related art shown in Fig. 2 is 0.80 μm, L_{iso} is sufficiently shorter than this and it is possible to shorten the distance L_p between the element isolation regions by using the gate electrode structure according to the above embodiment.

Fig. 5 is a sectional view of a semiconductor device having the gate electrode structure illustrated in Fig. 3 in A-A line direction illustrating another example of a semiconductor device of a structure enabling the width of the element isolation region to be shortened along with the shortening of the distance L_p between the PMOS formation region 4 and NMOS formation region 5.

In Fig. 5, an insulation film 21 is formed on the substrate 17, a PMOS substrate (or well) 18 is formed on the side of the insulation film 21 facing the PMOS

formation region, and an NMOS substrate (or well) 19 is formed on the side of the insulation film 21 facing the NMOS formation region.

The trench element isolation region is buried between the PMOS substrate (or well) 18 and NMOS substrate (or well) 19.

The p-type gate electrode 2 is formed on the PMOS substrate (or well) 18 through the insulation film 22, the n-type gate electrode 3 is formed on the NMOS substrate (or well) 19 through the insulation film, and the p-type impurity storage region 6, the n-type impurity storage region 8, and the polycrystalline silicon interconnection layer 10 are formed on the trench element isolation region 7.

The semiconductor device shown in Fig. 5 uses a silicon-on-insulator (SOI) structure where the PMOS substrate (or well) 18 and NMOS substrate (or well) 19 are formed on the insulation film 21.

In this structure, the PMOS substrate (or well) 18 and NMOS substrate (or well) 19 are completely insulated electrically by the trench element isolation region 7, so the element isolation performance is extremely high.

Further, the element isolation width L_{iso} in Fig. 5 can be expected to be close to the minimum fabricable

dimension in the element isolation structure.

For example, under the conditions of L_g = 0.20 μm, L_{ovlp} = 0.10 μm, and L_{diff} = 0.30 μm in the above embodiment, it is possible to make L_{iso} 0.20 μm or equal to the gate length L_g.

Accordingly, by using the gate electrode structure according to the above embodiment for that element isolation structure, it becomes possible to tremendously shorten the distance L_p between the PMOS and NMOS.

Summing up the effects of the invention, it becomes possible to suppress the lateral diffusion of gate impurities and to shorten the distance between the PMOS and NMOS and thereby to reduce the chip area.

While the invention has been described by reference to specific embodiments chosen for purposes of illustration, it should be apparent that numerous modifications could be made thereto by those skilled in the art without departing from the basic concept and scope of the invention.

What is claimed is:

1. A semiconductor device comprising:

a first element formation region in which a device of a first conductivity type is formed;

a second element formation region separated from said first element formation region by an element isolation region and in which a device of a second conductivity type different from said first conductivity type is formed;

a first gate electrode provided on said first element formation region and containing an impurity of the first conductivity type;

a second gate electrode provided on said second element formation region facing said first gate electrode and containing an impurity of the second conductivity type;

a first impurity storage region containing said first conductivity type impurity, having one end connected to an end of said first gate electrode, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes; and

a second impurity storage region containing said second conductivity type impurity, having one end connected to an end of said second gate electrode,

having the other end electrically connected to the other end of said first impurity storage region, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes.

2. A semiconductor device as set forth in claim 1, wherein said first and second impurity storage regions are physically connected to each other by a semiconductor layer.

3. A semiconductor device as set forth in claim 1, wherein the other ends of said first and second impurity storage regions are electrically connected to each other through a conductive layer.

4. A semiconductor device as set forth in claim 1, wherein said first and second impurity storage regions are arranged in a direction perpendicular to the direction of arrangement of said first and second gate electrodes.

5. A semiconductor device as set forth in claim 1, wherein said first and second gate electrodes and said first and second impurity storage regions are formed in the same conductive semiconductor layer.

6. A semiconductor device as set forth in claim 1, wherein said element isolation region is buried in a trench formed a boundary between said first and second conductive type of element formation regions in a

semiconductor substrate.

7. A semiconductor device as set forth in claim 1, wherein said element isolation region isolates first and second element formation regions comprised of semiconductor layers formed on an insulation layer.

8. A semiconductor device as set forth in claim 7, wherein said element isolation region is buried in a trench formed in said semiconductor layers.

9. A semiconductor device as set forth in claim 2, wherein:

said semiconductor layer is formed by polycrystalline silicon and

said first and second gate electrodes and first and second impurity storage regions are formed by selectively implanting impurities to said polycrystalline silicon layer.

10. A semiconductor device as set forth in claim 2, wherein the width of said semiconductor layer physically connecting said first and second impurity storage regions is a value allowing mask misalignment when forming said first and second gate electrodes and first and second impurity storage regions.

11. A semiconductor device as set forth in claim 1, wherein:

the widths of said first and second impurity

storage regions are equal to the gate length of said first and second gate electrodes and

the lengths of said first and second impurity storage regions are longer than said gate length.

SEMICONDUCTOR DEVICE

ABSTRACT OF THE DISCLOSURE

A semiconductor device suppressing the lateral diffusion of impurities doped in a PMOS and NMOS and shortening the distance between the PMOS and NMOS to reduce the size of the semiconductor device, including PMOS and NMOS formation regions isolated by an element isolation region; a p-type gate electrode arranged on the PMOS formation region; an n-type gate electrode arranged on the NMOS formation region; and first and second impurity storage regions arranged in a direction different from that of the arrangement of the p-type and n-type gate electrodes. An end of the first impurity storage region is connected to the p-type gate electrode, an end of the second impurity storage region is connected to the n-type gate electrode, and the other ends of the first and second impurity storage regions are electrically connected.

N98P1211US00

FIG. 1

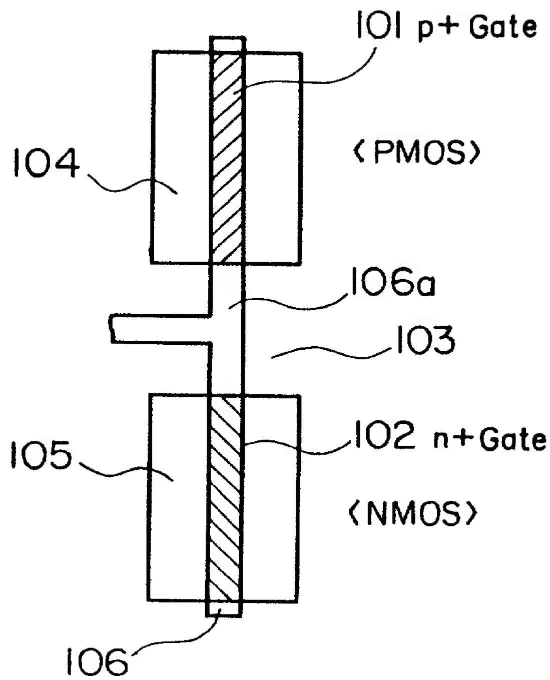


FIG. 2

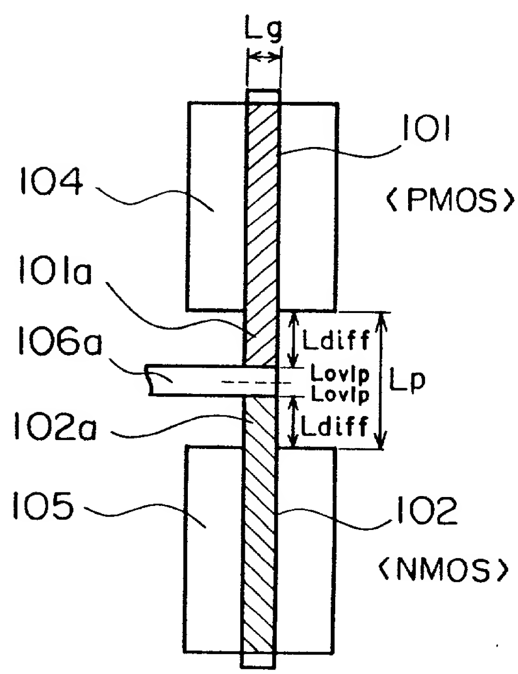


FIG. 3

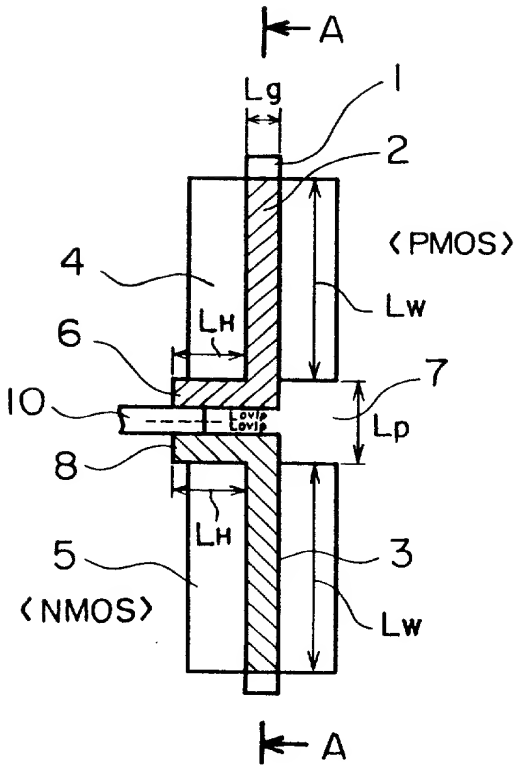


FIG. 4

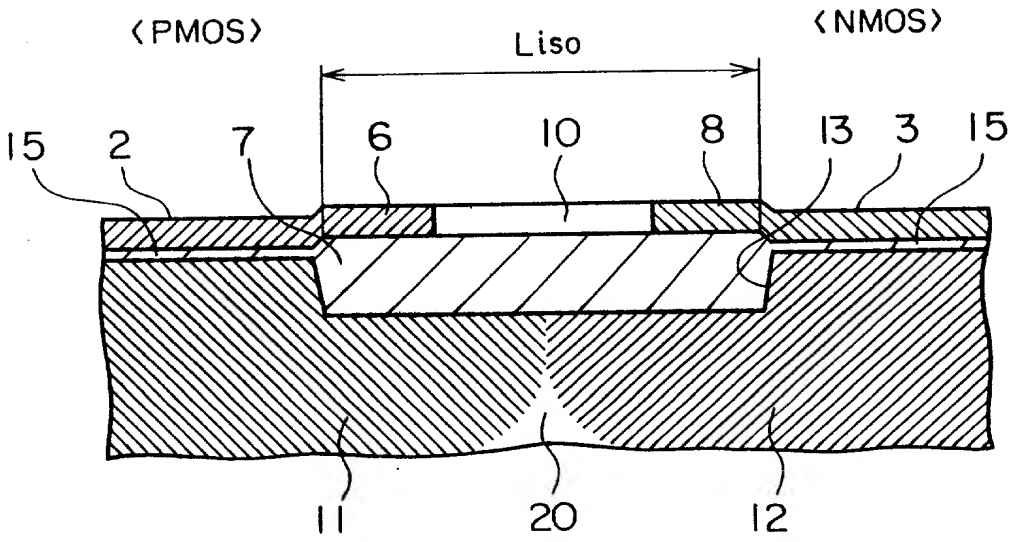
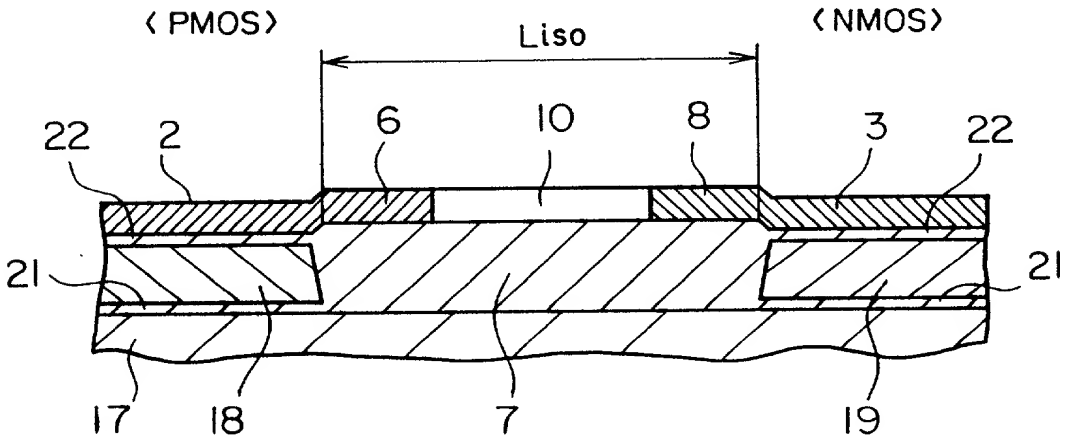

〈PMOS〉
Liso
〈NMOS〉
15
2
7
6
10
8
13
3
15
11
20
12

FIG. 5


〈PMOS〉
Liso
〈NMOS〉
22
2
6
10
8
3
22
21
21
17
18
7
19

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICE

Case No. P98,2413 *, the specification of which*

	X	*is attached hereto.*
(check	___	*was filed on* _____, *as*
one)		*Application Serial No.* _____
		and was amended on _____.
		(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent Office all information which is known to me to be material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, 1.56(a).[1]

I do not know and do not believe this invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and I believe that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as identified below:

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below

Prior Foreign Application(s)

Number	*Country*	*Date*
P09-345363	Japan	December 15, 1997

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[1] *(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and*

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the above listed application on which priority is claimed:

Prior Foreign Application(s)

Number	*Country*	*Date*

If no priority is claimed, I have identified all foreign patent applications filed prior to this application:

Prior Foreign Application(s)

Number	*Country*	*Date*

And I hereby appoint Messrs. John D. Simpson (Registration No. 19,842), Lewis T. Steadman (17,074), Dennis A. Gross (24,410), Steven H. Noll (28,982), Thomas I. Ross (29,275), Kevin W. Guynn (29,927), Robert M. Barrett, (30,142), Robert M. Ward (26,517), Brett A. Valiquet (27,841), Edward A. Lehman (22,312), James D. Hobart (24,149), Marvin Moody (16,549), Melvin A. Robinson (31,870), David R. Metzger (32,919), John R. Garrett (27,888), James Van Santen (16,584), William C. Stueber (16,453), and J. Arthur Gross (13,615) all members of the firm of Hill, Steadman & Simpson, A Professional Corporation
Telephone: 312/876-0200 Ext. _____
my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and direct that all correspondence be forwarded to:

Hill, Steadman & Simpson
A Professional Corporation
85th Floor Sears Tower, Chicago, Illinois 60606

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature Hajime Nakayama *Date* December 3, 1998
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